REMARKS

This response is being filed as part of a Request for Continued Examination pursuant to 37 C.F.R. § 1.114, and is intended to be completely responsive to the Final Office Action dated September 23, 2004 and the Advisory Action dated December 28, 2004 concerning the above-referenced patent application. The Applicants note that the amendments filed November 22, 2004 were refused entry.

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow. Claims 1-4 and 6-20 have been rejected and Claim 5 has been objected to by the Examiner. Claims 1, 5, 11, and 17 have been amended, and new Claim 21 has been added. No new matter has been added. Accordingly, Claims 1-21 will be pending in the present application upon entry of this Reply and Amendment.

The title has been amended to read as follows: OFFSET SPACER PROCESS FOR FORMING N-TYPE TRANSISTORS.

A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

Claim Objections, Comment on Statement of Reasons for Allowance, and New Claim 21

On page 9 of the Office Action, the Examiner indicated that Claim 5 was objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Claim 5 has been rewritten in independent form including all of the limitations of Claims 1-4. Reconsideration and allowance of Claim 5 is respectfully requested.

While the Applicants agree that allowed Claims 5 as amended recites a combination of subject matter that is patentable over the cited references, the Applicants do not necessarily agree with or acquiesce in the statement of reasons for allowance given by the Examiner. Moreover, the Applicants note that the recited subject matter as well as various other subject

matter and/or combinations of subject matter may be patentable for other reasons than those given by the Examiner. The Applicants expressly reserve the right to set forth additional and/or alternative reasons for patentability and/or allowance with the present Application or in any other future proceeding.

The Applicants submit that new Claim 21 is allowable over the references cited by the Examiner. The Examiner indicated that the "primary reason for the indication of allowable subject matter of claim 5 is the inclusion therein, in combination as currently claimed, of the limitation of forming both the first and second spacers of nitride." New Claim 21 is presented as including all limitations of independent Claim 1 and dependent Claim 5. The Applicants note that Claim 5 as amended differs from new Claim 21 in that Claim 5 includes limitations from Claims 2, 3, and 4 which are not included in new Claim 21. The Applicants believe that new Claim 21 is allowable over the references cited by the Examiner for at least the reason that the limitation of forming both the first and second spacers of nitride is included in new Claim 21.

Claim Rejections – 35 U.S.C. § 103

1. Claims 1-4, 7-10, and 17-20 (Zheng et al. and Chu et al.)

On page 2 of the Office Action, Claims 1-4, 7-10, and 17-20 were rejected as being unpatentable over U.S. Patent No. 6,762,085 to Zheng et al. in view of U.S. Patent No. 6,649,492 to Chu et al. under 35 U.S.C. § 103(a). The Applicants respectfully traverse these rejections.

Claim 1 (as amended) recites "selectively providing a second spacer to the first gate structure; and forming second deep source and drain regions in the strained semiconductor layer in the first area after the step of selectively providing a second spacer to the first gate structure" (emphasis added).

Claim 17 (as amended) recites "selectively providing spacers for the first set of gate structures; and forming deep source and drain regions on each side of the first set of the gate structures after selectively providing spacers for the first set of gate structures (emphasis added)."

Neither Zheng et al. nor Chu et al., whether taken alone or in proper combination, teach or suggest forming source and drain regions after selectively providing spacers for a first gate structure (or set of gate structures). In contrast, Zheng et al. shows in Figures 5-7 (described at columns 3-4 of Zheng et al.) the formation of, for example, "halo, LDD regions, and heavily doped source/drain regions" before formation of "silicon nitride shapes 14b."

As described with respect to one exemplary embodiment at pages 8-9, paragraph [0030] of the present application (with emphasis added):

> **[0030]** Process 100 can be utilized to form integrated circuit 12. According to process 100, integrated circuit 12 is formed by providing source and drain regions 22B and 24B (for NMOS) after an offset spacer is provided. The offset spacer increases the distance between regions 22B and 24B and an edge of gate conductor 46B. The increased distance compensates for the enhanced lateral diffusion of arsenic (As) dopants which are particularly problematic for NMOS transistors formed on strained layers. Regions 22A and 24A for PMOS transistors are formed without a second spacer or an offset spacer because diffusion of P-type dopants such as boron (B) is suppressed in strained layers.

The fact that such "halo, LDD regions, and heavily doped source/drain regions" in Zheng et al. are formed before formation of "silicon nitride shapes 14b" indicates that the "silicon nitride shapes 14b" of Zheng et al. do not compensate for lateral diffusion of dopants during doping operations. It should also be noted that Chu et al. does not provide the necessary teaching or suggestion of forming source and drain regions after selectively providing spacers for a first gate structure or field effect transistors (or set of gate structures).

Accordingly, the rejections of Claims 1-4, 7-10, and 17-20 should be withdrawn, because the combination of Zheng et al. and Chu et al. fails to teach at least one limitation of each of rejected independent Claims 1 and 17. Reconsideration and withdrawal of the rejections of Claims 1-4, 7-10, and 17-20 under 35 U.S.C. § 103(a) is therefore respectfully requested.

2. Claims 11 and 14-16 (Haken and Chu et al.)

On page 4 of the Office Action, Claims 11 and 14-16 were rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 5141890 to Haken in view of U.S. Patent No. 6,649,492 to Chu et al. Applicants respectfully traverse this rejection.

Independent Claim 11 (as amended) recites, among other limitations, "selectively providing offset spacers adjacent the spacers of a second group of the field effect transistors."

One exemplary embodiment showing the provision of an offset spacer adjacent spacers of a field effect transistor is shown in Figure 5 of the present application, which illustrates a spacer 43 provided adjacent a spacer 33B. Neither Haken nor Chu et al., alone or in proper combination, teach or suggest providing offset spacers adjacent spacers of a field effect transistor. For example, as shown in Figure 3 of Haken, only a single "sidewall oxide" is provided in the left-most transistor shown. There is no teaching or suggestion in Haken that an offset spacer may be provided adjacent the "sidewall oxide," nor does there appear to be any recognition of the benefits of providing such an offset spacer.

The method recited in independent Claim 11, considered as a whole, would not have been obvious in view of Haken and Chu et al., because at least one limitation recited in Claim 11 is not taught or suggested by the combination of Haken and Chu et al. The Applicants respectfully request reconsideration withdrawal of the rejection of independent Claim 11 and dependent Claims 14-16 under 35 U.S.C. § 103(a).

3. Claim 12 (Haken, Chu et al., and Sitaram et al.)

On page 6 of the Office Action, Claim 12 was rejected under 35 U.S.C. § 103(a) as being obvious in view of Haken in view of Chu et al. and further in view of U.S. Patent No. 5,384,285 to Sitaram et al. Applicants respectfully traverse this rejection.

Claim 12 depends from independent Claim 11 (as amended), which recites, among other limitations, "selectively providing offset spacers adjacent the spacers of a second group of the field effect transistors."

As noted above, neither Haken nor Chu et al., alone or in proper combination, teach or suggest the provision of offset spacers adjacent spacers of a group of field effect transistors. Sitaram et al. also does not teach or suggest such a limitation. For example, no offset spacer is provided adjacent the "insulating side wall spacer 26" shown in Figure 4 of Sitaram et al., nor is there any teaching or suggestion that it would be possible or desirable to do so (it should be noted that Figures 2 and 3 show the provision of a "transition-metal layer 30" and a "capping layer 32," neither of which are "offset spacers" as that term is used in independent Claim 11).

The rejection of Claim 12 should be withdrawn, because at least one limitation of independent Claim 11 (and of corresponding dependent Claim 12) is not taught or suggested by the combination of Haken, Chu et al., and Sitaram et al. Accordingly, the Applicants request reconsideration and withdrawal of the rejection of Claim 12 under 35 U.S.C. § 103(a).

4. Claim 13 (Haken, Chu et al., Sitaram et al., and Blair et al.)

On page 6 of the Office Action, Claim 13 was rejected under 35 U.S.C. § 103(a) as being obvious in view of Haken, in view of Chu et al. and Sitaram et al. and further in view of U.S. Patent No. 5,998,873 to Blair et al. Applicants respectfully traverse this rejection.

Claim 13 depends from independent Claim 11 (as amended), which recites, among other limitations, "selectively providing offset spacers adjacent the spacers of a second group of the field effect transistors."

As noted above, the combination of Haken, Chu et al., and Sitaram et al. does not teach or suggest the provision of offset spacers adjacent spacers of a group of field effect transistors. Blair et al. also does not teach or suggest such a limitation. For example, no offset spacers are provided adjacent the "gate sidewall spacers 308 and 310" shown in Figure 5 of Blair et al., nor is there any teaching or suggestion that it would be possible or desirable to do so.

The rejection of Claim 13 should be withdrawn, because at least one limitation of independent Claim 11 (and of corresponding dependent Claim 13) is not taught or suggested by the combination of Haken, Chu et al., Sitaram et al., and Blair et al. Accordingly, the

Applicants request reconsideration and withdrawal of the rejection of Claim 13 under 35 U.S.C. § 103(a).

5. Claims 1, 7, 8, and 17 (Kim et al. and Chu et al.)

On page 7 of the Office Action, Claims 1, 7, 8, and 17 were rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 5,291,052 to Kim et al. in view of Chu et al. Applicants respectfully traverse this rejection.

Claim 1 (as amended) recites (with emphasis added), "selectively providing a second spacer to the first gate structure; and forming second deep source and drain regions in the strained semiconductor layer in the first area; wherein the first gate structure is part of an NMOS transistor and the second gate structure is part of a PMOS transistor."

Claim 17 (as amended) recites (with emphasis added), "covering a first set of gate structures that are part of NMOS transistors; forming deep source and drain regions on each side of a second set of the gate structures that are part of PMOS transistors...selectively providing spacers for the first set of gate structures; and forming deep source and drain regions on each side of the first set of the gate structures."

One exemplary embodiment is described at paragraph [0030] of the present application as follows (with emphasis added):

> Process 100 can be utilized to form integrated circuit 12. according to process 100, integrated circuit 12 is formed by providing source and drain regions 22B and 24B (for NMOS) after an offset spacer is provided. The offset spacer increases the distance between regions 22B and 24B and an edge of gate conductor 46B. The increased distance compensates for the enhanced lateral diffusion of arsenic (As) dopants which are particularly problematic for NMOS transistors formed on strained layers. Regions 22A and 24A for PMOS transistors are formed without a second spacer or an offset spacer because diffusion of P-type dopants such as boron (B) is suppressed in strained layers.

In contrast to the subject matter recited in independent Claims 1 and 17 in which a second spacer is provided for gate structures that are part of NMOS transistors (Claim 1) or in

which a spacer is provided for a first set of gate structures that are part of NMOS transistors (Claim 17), Kim et al. describes the use of a "second gate side wall spacer 15a" that is provided for a PMOS transistor (see, e.g., column 3, lines 48-52 and column 5, lines 40-58). Kim et al. thus uses the "second gate side wall spacer 15a" with a PMOS transistor instead of with an NMOS transistor.

There is no teaching or suggestion in Kim et al. (or in Chu et al.) to use a "second spacer" as recited in Claim 1 or a "spacer" as recited in Claim 17 with an NMOS transistor. The Applicants have recognized a need with NMOS transistors (e.g., compensation for enhanced lateral diffusion of n-type dopants in strained semiconductor layers) that is not appreciated by the teachings of Kim et al. or Chu et al. As noted by the Examiner, "[Kim et al.] does not disclose that the substrate includes a strained semiconductor layer." As a result, there is no indication that Kim et al. appreciates the teaching of paragraph [0030] of the present application, which states with regard to the exemplary embodiment described that "PMOS transistors are formed without a second spacer or an offset spacer because diffusion of P-type dopants such as boron (B) is suppressed in strained layers" (emphasis added). Since Kim et al. does not disclose a strained semiconductor layer, it is clear that this reference does not appreciate the use of spacers such as those recited in Claims 1 and 17 for use with NMOS spacers.

The rejection of Claims 1, 7, 8, and 17 should be withdrawn, because at least one limitation of independent Claims 1 and 17 (and corresponding dependent Claims 7 and 8) is not taught or suggested by the combination of Kim et al. and Chu et al. The Applicants request reconsideration and withdrawal of the rejection of Claims 1, 7, 8, and 17 under 35 U.S.C. § 103(a).

6. Claim 6 (Kim et al., Chu et al., and Sitaram et al.)

On page 8 of the Office Action, Claim 6 was rejected under 35 U.S.C. § 103(a) as being obvious over Kim et al. in view of Chu et al. and further in view of Sitaram et al. Applicants respectfully traverse this rejection.

As described in the preceding section, the combination of Kim et al. and Chu et al. does not teach or suggest the use of a "second spacer" such as that recited in Claim 1 (from which Claim 6 depends) with a gate structure of an NMOS transistor. Because Sitaram et al. does not teach or suggest the use of a "second spacer" (see, e.g., the single "insulating side wall spacer 26 shown in Figure 4 of Sitaram et al.), this reference also does not teach or suggest the use of a second spacer with a gate structure of an NMOS transistor, either alone or in combination with Kim et al. and Chu et al.

The rejection of Claim 6 should be withdrawn, because at least one limitation of independent Claim 1 is not taught or suggested by the combination of Kim et al., Chu et al., and Sitaram et al. The Applicants request reconsideration and withdrawal of the rejection of Claim 6 under 35 U.S.C. § 103(a).

* * *

It is submitted that each outstanding objection and rejection to the Application has been overcome, and that the Application is in a condition for allowance. The Applicants request consideration and allowance of all pending Claims 1-20.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

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